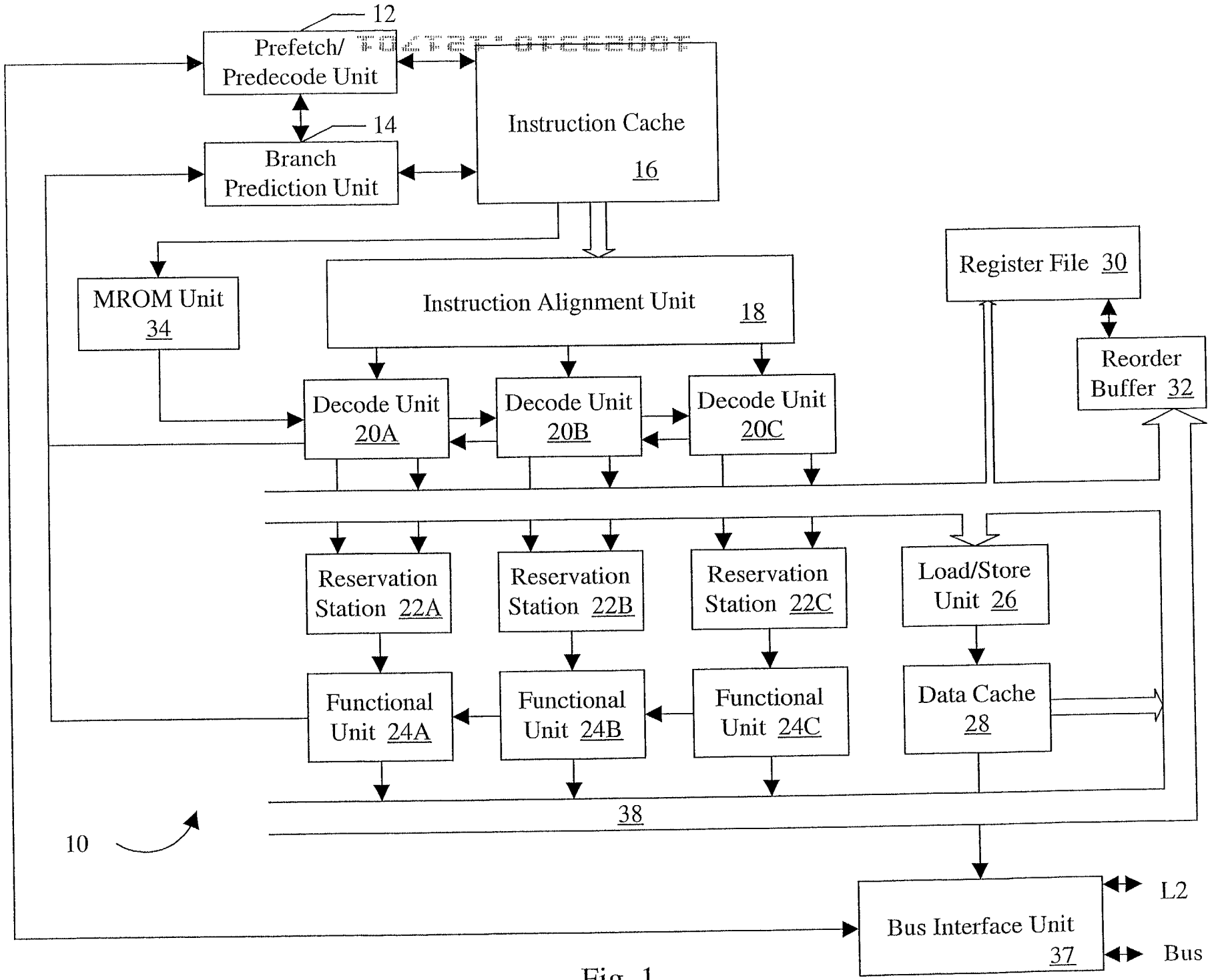
12
Prefetch/
Predecode Unit
14
Branch
Prediction Unit
Instruction Cache
16
MROM Unit
34
Instruction Alignment Unit
18
Register File 30
Reorder
Buffer 32
Decode Unit
20A
Decode Unit
20B
Decode Unit
20C
Reservation
Station 22A
Reservation
Station 22B
Reservation
Station 22C
Load/Store
Unit 26
Functional
Unit 24A
Functional
Unit 24B
Functional
Unit 24C
Data Cache
28
38
10
Bus Interface Unit
37
L2
Bus

Fig. 1

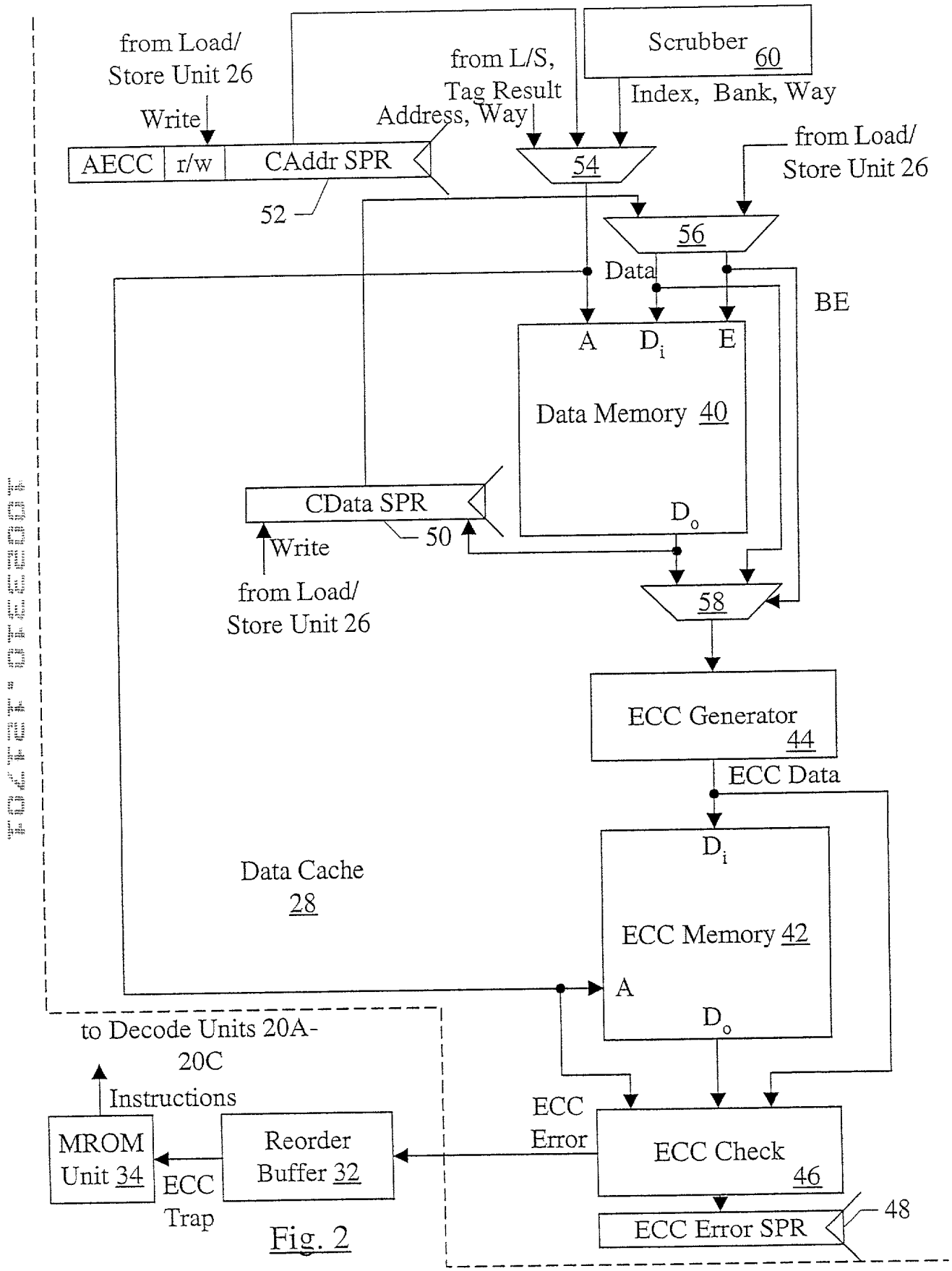
from Load/
Store Unit 26
Write
from L/S,
Tag Result
Address, Way
Scrubber 60
Index, Bank, Way
AECC
r/w
CAddr SPR
52
54
from Load/
Store Unit 26
56
Data
BE
A
D_i
E
Data Memory 40
CData SPR
50
D_o
Write
from Load/
Store Unit 26
58
ECC Generator
44
ECC Data
D_i
Data Cache
28
ECC Memory 42
A
D_o
to Decode Units 20A-
20C
Instructions
MROM
Unit 34
ECC
Trap
Reorder
Buffer 32
ECC
Error
ECC Check
46
ECC Error SPR
48

Fig. 2

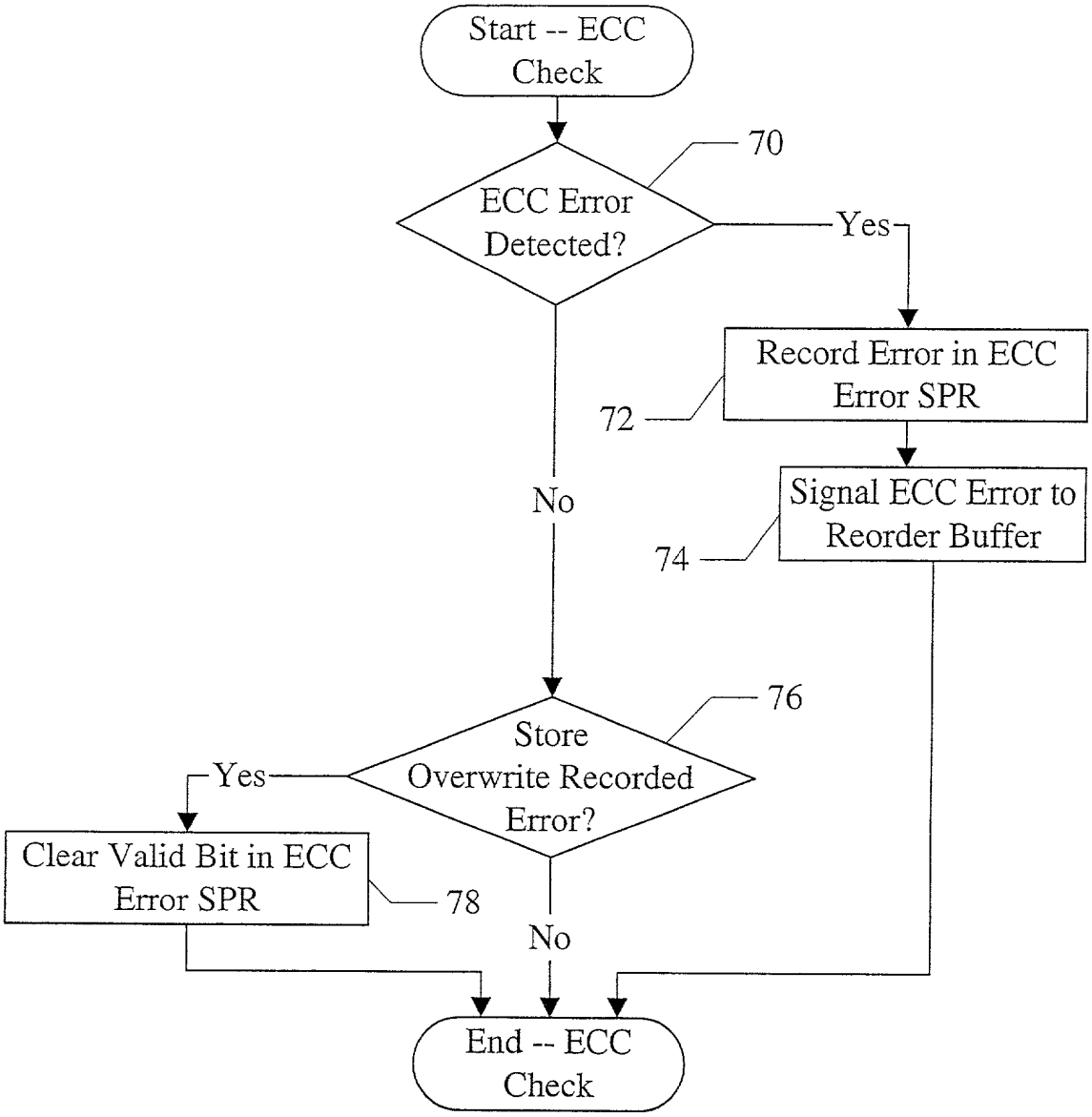
Start -- ECC Check
70
ECC Error Detected?
Yes
Record Error in ECC Error SPR
72
Signal ECC Error to Reorder Buffer
74
No
76
Store Overwrite Recorded Error?
Yes
Clear Valid Bit in ECC Error SPR
78
No
End -- ECC Check

Fig. 3

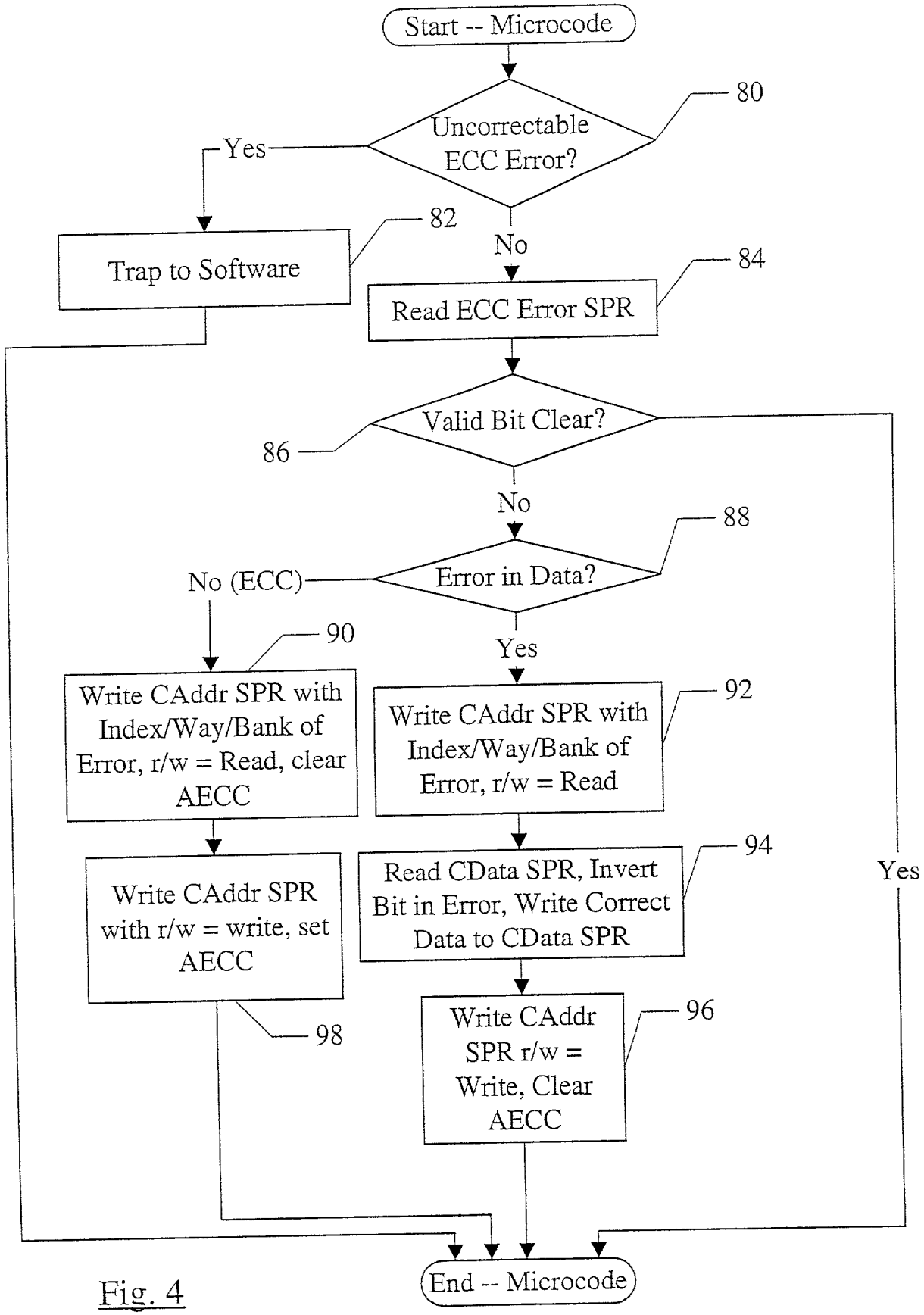
Start -- Microcode
Uncorrectable ECC Error?
80
Yes
No
Trap to Software
82
Read ECC Error SPR
84
Valid Bit Clear?
86
No
Error in Data?
88
No (ECC)
Yes
Write CAddr SPR with Index/Way/Bank of Error, r/w = Read, clear AECC
90
Write CAddr SPR with Index/Way/Bank of Error, r/w = Read
92
Write CAddr SPR with r/w = write, set AECC
Read CData SPR, Invert Bit in Error, Write Correct Data to CData SPR
94
Yes
98
Write CAddr SPR r/w = Write, Clear AECC
96
End -- Microcode

Fig. 4

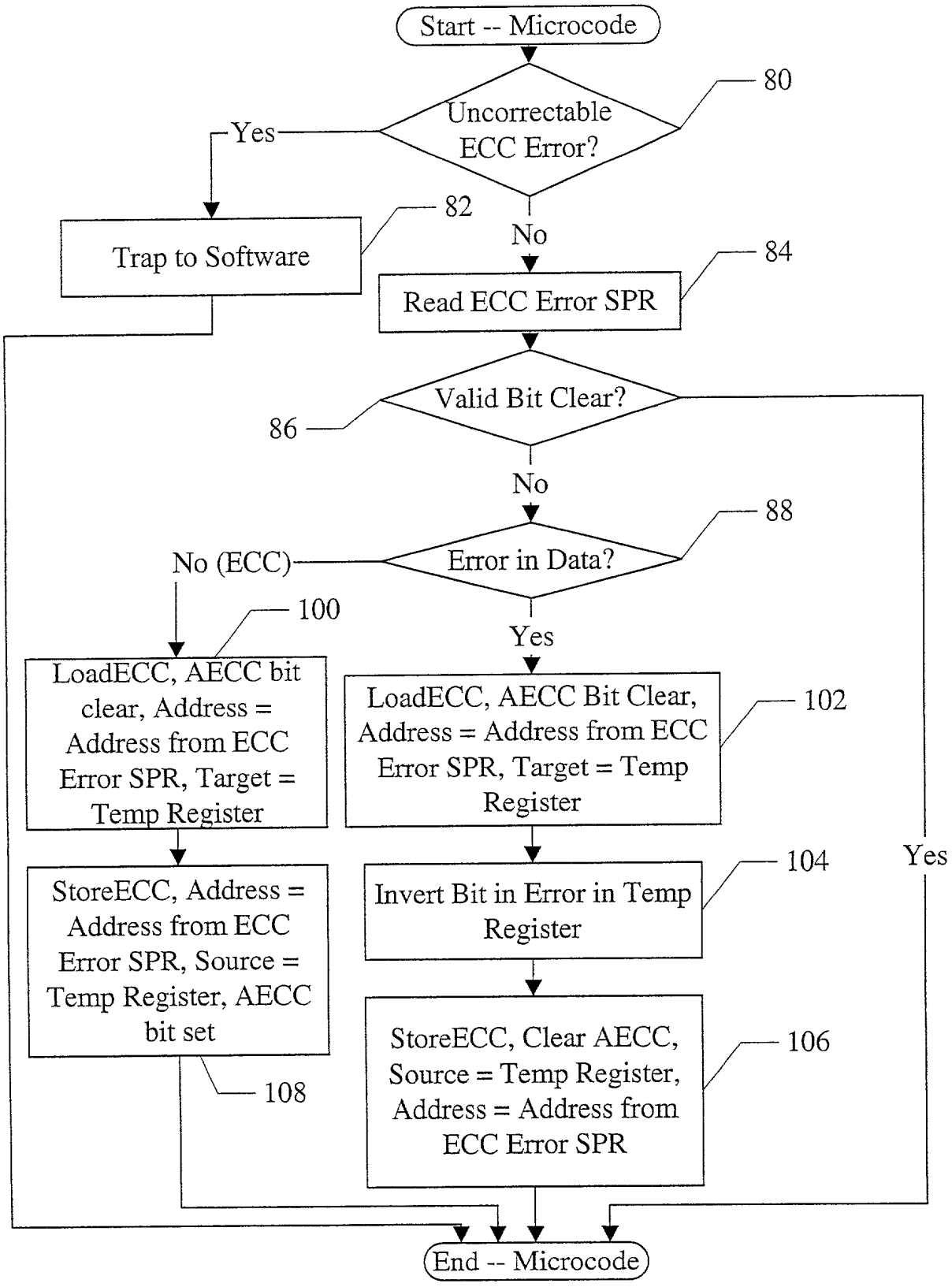
Start -- Microcode
Uncorrectable ECC Error?
80
Yes
No
Trap to Software
82
Read ECC Error SPR
84
Valid Bit Clear?
86
No
Error in Data?
88
No (ECC)
Yes
100
LoadECC, AECC bit clear, Address = Address from ECC Error SPR, Target = Temp Register
LoadECC, AECC Bit Clear, Address = Address from ECC Error SPR, Target = Temp Register
102
StoreECC, Address = Address from ECC Error SPR, Source = Temp Register, AECC bit set
Invert Bit in Error in Temp Register
104
Yes
108
StoreECC, Clear AECC, Source = Temp Register, Address = Address from ECC Error SPR
106
End -- Microcode

Fig. 5

V	Index	Way	Bank	Error Bit	ECC/Data

Fig. 6

V	Address	Error Bit	ECC/Data

Fig. 7

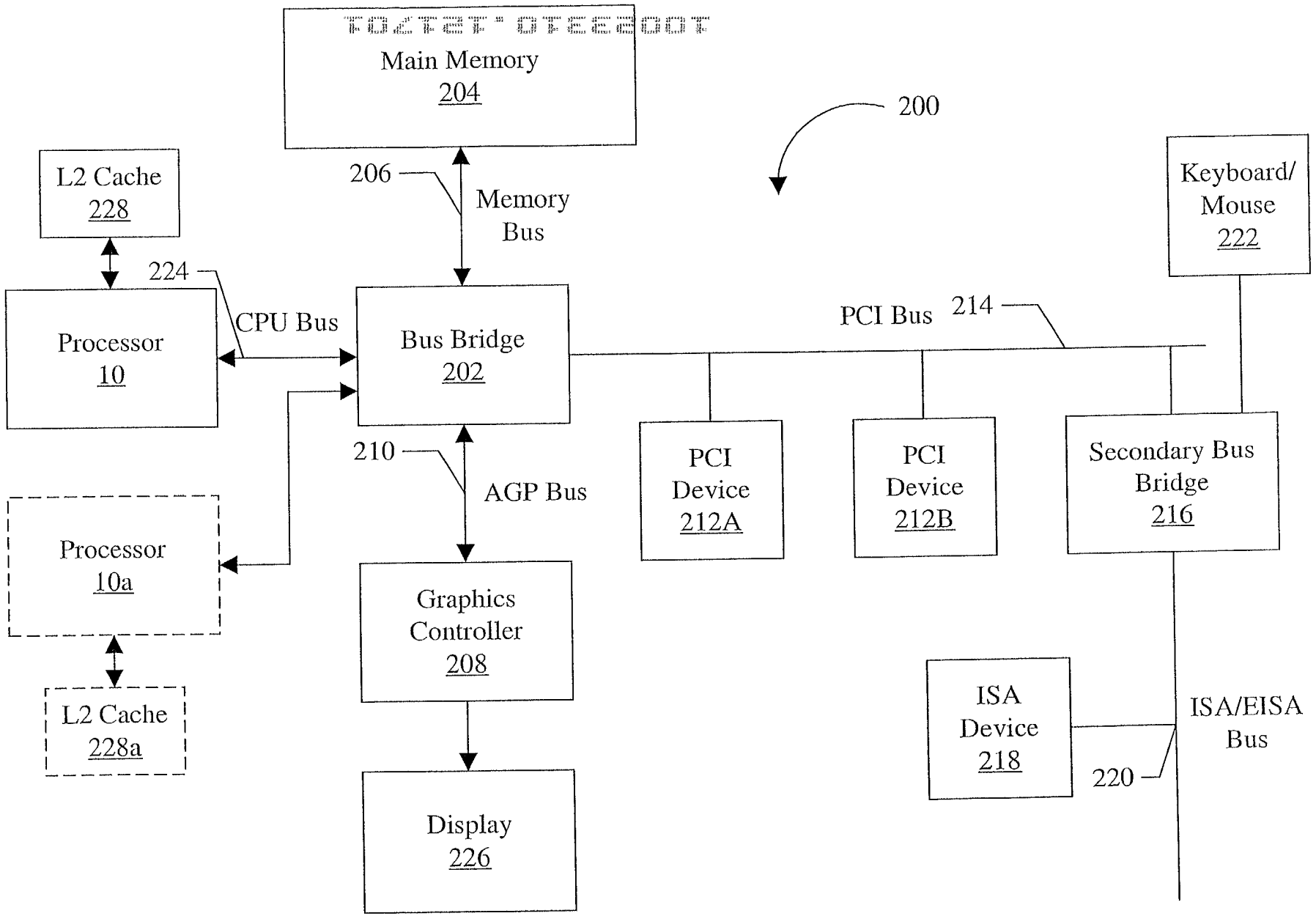
Main Memory
204
200
L2 Cache
228
206
Memory
Bus
Keyboard/
Mouse
222
224
CPU Bus
Processor
10
Bus Bridge
202
PCI Bus
214
210
AGP Bus
PCI
Device
212A
PCI
Device
212B
Secondary Bus
Bridge
216
Processor
10a
Graphics
Controller
208
ISA
Device
218
ISA/EISA
Bus
220
L2 Cache
228a
Display
226

Fig. 8

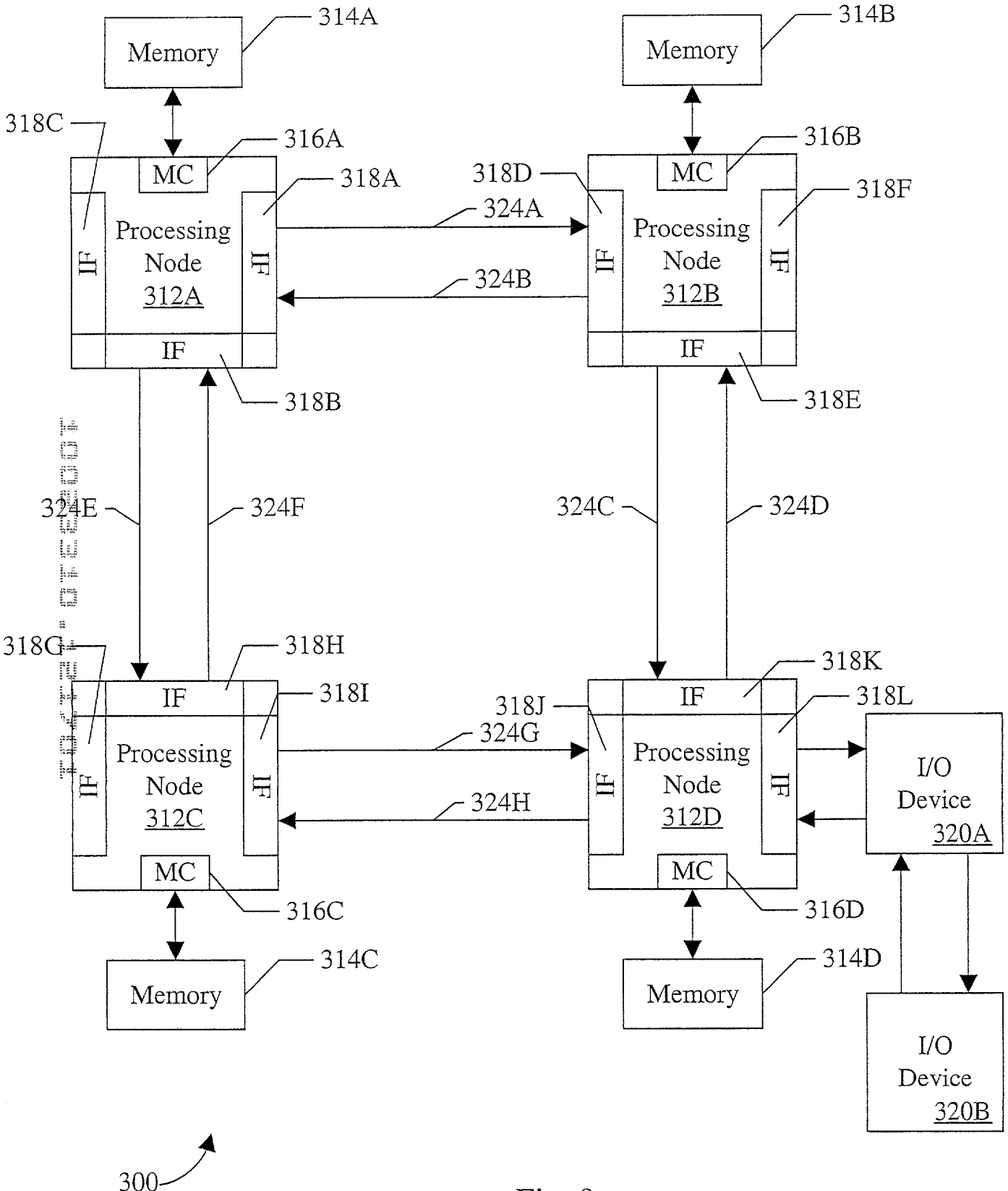
Memory
314A
Memory
314B
318C
316A
MC
318A
318D
316B
MC
318F
324A
Processing Node 312A
IF
IF
IF
324B
Processing Node 312B
IF
IF
IF
318B
318E
324E
324F
324C
324D
318G
318H
318K
IF
318I
318J
IF
318L
324G
Processing Node 312C
IF
IF
IF
324H
Processing Node 312D
IF
IF
I/O Device 320A
MC
316C
MC
316D
Memory
314C
Memory
314D
I/O Device 320B
300

Fig. 9